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Microwave properties of $SrTiO_3/SrRuO_3/CeO_2/YSZ$ heterostructure on low-resistivity silicon

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Abstract

Properties of thin film $SrTiO_3/SrRuO_3/CeO_2/YSZ$ heterostructures on low-resistivity (25 Ωcm) Si substrates are studied at microwave frequencies. Heterostructures are grown by laser ablation at different conditions and characterized by XRD. Coplanar capacitors with 2 μm gap are formed by a lift-off process of the Au/Ti electrodes deposited by e-beam evaporation on the surface of heterostructures. Microwave properties of the capacitors are measured at room temperature in the range of 1–50 GHz as a function of electric field. The measured tunability of the capacitors is in the range of 10–20%. The loss in capacitors is caused mainly by the Si substrate with maximum value around the dielectric relaxation frequency 6 GHz. The intrinsic loss tangent (0.08 at 50 GHz) of capacitors is calculated from equivalent circuit model by removing the substrate loss.

Keywords: Capacitors; Dielectric properties; $SrTiO_3$

1. Introduction

Strontium-titanate, $SrTiO_3$ (STO), or a solid solution of $Ba_{1-x}Sr_xTiO_3$ (BSTO), are being investigated as dielectric material for tunable microwave applications.[1–4] The electric field-dependent dielectric permittivity can be utilized in devices such as varactors, tunable oscillators, phase shifters, etc.[1,5,6] Usually these devices require high tunability of permittivity and low dielectric loss. It is important, from an industrial respective, to integrate these devices with the Si substrate since microwave ICs are going to heavily rely on Si technology. However, the resistivity of common CMOS grade silicon wafers is rather low (in the range of 1–25 Ω cm) that causes high microwave loss in circuit elements placed directly on Si substrates. A number of methods have been developed to solve this problem. The first approach is to use commercially available high resistive Si wafers (up to 10 kΩ cm) since all circuit components may be implemented in the same way as they are on semi-insulating GaAs, InP, or ceramic substrates.[4,7] Another approach is to form the circuit elements directly on low resistivity Si and then to remove the Si areas below the elements using micromachining techniques.[8]

In this paper we present the results of preparation and the microwave study of a heterostructure, incorporating STO thin film, on low resistivity Si ($\rho = 25$ Ω cm). In order to provide the epitaxial growth and improved dielectric properties of STO layer we grew a $SrRuO_3/CeO_2/YSZ$ buffer thin film structure between STO and the Si substrate.[9,10,11]

2. Experimental

2.1. Sample preparation

The $SrTiO_3/SrRuO_3/CeO_2/YSZ$ and CeO_2/YSZ heterostructures were grown in situ by pulsed laser deposition technique on *n*-type Si(100) substrates ($\rho = 25$ Ω cm) with native SiO_2 layer. A beam of KrF excimer laser ($\lambda = 248$ nm, $\tau = 30$ ns) operating at 10 Hz with energy density of 1.5 J cm^{-2} was used to ablate the stoichiometric targets. An on-axis deposition configuration with target-to-substrate distance of 5 cm was used. The substrates are fixed to the surface of resistive heater with silver glue. The growth temperature of each layer was optimized for crystal quality of STO layer (intensity

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and rocking curve of XRD ω-scans). The growth temperature, thickness of layers and bulk lattice parameters of materials are presented in Table 1. In order to avoid further growth of the SiO_2 on the Si wafer, no oxygen was introduced into the vacuum chamber during the deposition of the first YSZ buffer layer.[9,12] The oxygen pressure during deposition of CeO_2, $SrRuO_3$ and STO layers was 0.4 mbar. After deposition, the samples were cold down to room temperature at oxygen pressure of 400 mbar.

Coplanar capacitor $SrTiO_3/SrRuO_3/CeO_2$/YSZ test structures were formed by a lift-off process of e-beam evaporated Au (≈0.5 μm)/Ti (20 nm) film electrodes. The cross section view of a capacitor test structure presented in Fig. 1(a). The electrodes have rectangular shape with lateral sizes of 150×125 μm^2. The straight gap (g) between electrodes is 2 μm. The planar design (Refs. 1, 3 and 7) used in this work is simple in fabrication, on-wafer characterization and suitable for integration with microwave integrated circuits. The $SrRuO_3$ layer is rather thin (50 nm) and its sheet resistance is high (50 Ω/square). For this reason the microwave field penetrates the silicon substrate and experiences some losses. Special CeO_2/YSZ open structure with identical geometry of electrodes were fabricated and used for measurement of the losses associated with the silicon substrate. The cross sectional view of a capacitor open structure is presented in Fig. 1(b).

2.2. Sample characterization

The microstructure of the layers were characterized by normal θ–2θ and ω-scan XRD patterns measured using a Philips X'pert SW 3040 equipped by MRD lens and point Cu $K_{\alpha 1}$, $K_{\alpha 2}$ and K_{β} radiation source.

The dielectrical properties of the test and open structures were studied using HP8510C vector network analyser and a standard probe station S-1160 Signatone with microprobes (Fig. 1). The real, ReY, and imaginary, ImY, parts of complex admittance Y, of the structures were extracted directly from an inverted Smith chart. The capacitance C, conductivity G and effective loss tangent $tan\delta$ were computed using Eqs. (1) and (2):

$$Y = ReY + ImY = G + j\omega C, \tag{1}$$

$$\tan\delta = ReY/\ ImY \tag{2}$$

where ω is the angular frequency. In the measurements, the maximum level of microwave power delivered to the device under test is $P = 1$ mW, and the amplitude of the microwave signal is estimated to be $V_{ac} = \sqrt{2Z_0P} = 0,3$V ($Z_0 = 50$ Ω is the characteristic impedance of the transmission line), that is still low enough to cause substantial nonlinearities in the STO film. In measurements the dc bias V is reversed periodically to enable plots of the hysteresis effects in $C-V$ performance. The tunability of test structure is defined as $T(V) = [C(0)-C(V)]/C(0)$, where $C(0)$ and $C(V)$ are capacitances without and with dc bias, respectively.

Table 1
Growth temperature T_d, thickness t of layers and bulk lattice parameters of materials a

Layer	YSZ	CeO_2	$SrRuO_3$	$SrTiO_3$
T_d, °C	770	720	780	700
t, nm	50	10	50	100
a, nm	0.514	0.541	0.393	0.3905

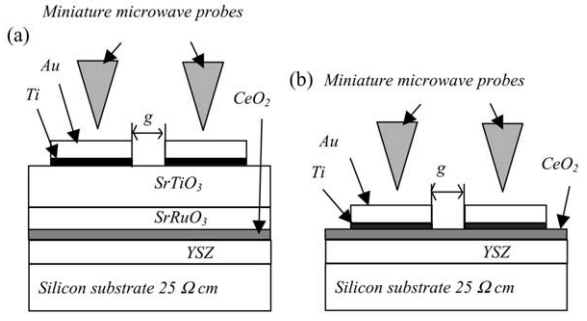

Fig. 1. Cross section view of a capacitor $SrTiO_3/SrRuO_3/CeO_2$/YSZ/Si test structure (a) and CeO_2/YSZ/Si open structure (b).

3. Results and discussion

3.1. Microstructure

The normal XRD θ–2θ scans of $SrTiO_3/SrRuO_3/CeO_2$/YSZ/Si heterostructures in the range of 20–120° reveal reflections associated only with SRO{110}, STO{110} and YSZ{001} families of planes. The CeO_2{001} peaks are, probably, masked by STO{110} due to smaller thickness of CeO_2 layer.[13] Fig. 2 shows the 30–36° range θ–2θ scans of heterostructures obtained at different growth temperatures of $SrTiO_3$ ($T_{d\ STO} = 650$ and 700 °C). In order to identify the SRO and STO peaks, we compared the scans at different $T_{d\ STO}$. As it can be seen, the increase of $T_{d\ STO}$ causes approximately a 10 times increase of intensity of the peak at $2\theta \approx 33.2°$, which allows us to consider this peak as STO(110). The 2θ-position of YSZ(002) ($2\theta \approx 35°$) is in agreement with Refs. 10 and 13 and corresponds to the unstrained bulk lattice parameter (Table 1). Using the method of analysis of strained epitaxial film microstructure (Ref. 14) we calculated YSZ(002) position $2\theta \approx 36°$ for the coherent growth case. It indicates that YSZ grows incoherently on the Si substrate. The inset in Fig. 2 shows FWHM values of the ω scans of YSZ, SRO, and STO layers for $T_{d\ STO} = 700$ °C. The FWHM values of all layers are less than 1°, which indicates the good structural epitaxial growth.[10]

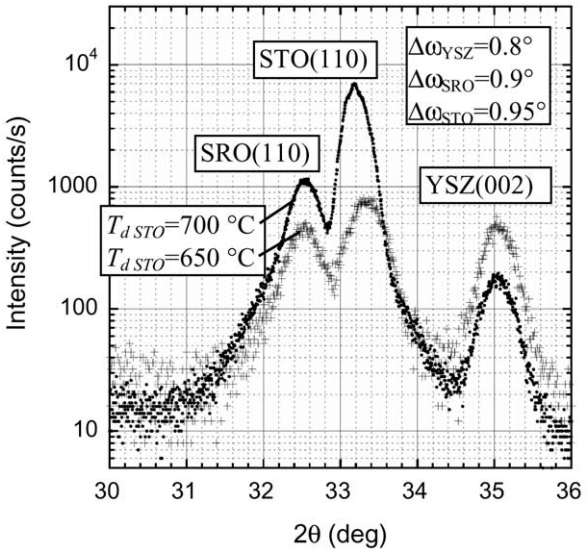

Fig. 2. The normal θ–2θ XRD scans of $SrTiO_3/SrRuO_3/CeO_2/YSZ/Si$ heterostructures obtained at different growth temperatures of $SrTiO_3$ layer: $T_{d\ STO}=650$ and 700 °C. The inset shows FWHM values of the ω scans of YSZ, SRO, and STO layers for $T_{d\ STO}=700$ °C.

3.2. Equivalent circuit

It is convenient to study the dielectric properties of the test structures using parallel equivalent circuits shown in Fig. 3(a). Here the capacitance between the electrodes due to the in-plane orientation of the STO film is denoted by C_{ab}. C_{C1} and C_{C2} are the equivalent capacitances between the electrodes and SRO layer associated with the out-of-plane orientation of the STO film. The C_{ox1} and C_{ox2} capacitances are associated with CeO_2/YSZ oxide layers between the SRO film and Si substrate. Due to shorting out by $SrRuO_3$ layer (sheet resistance $\sim$50 Ω/square)[15] the static field does not penetrate the Si substrate. However, a time-varying field penetrates the SRO layer (skin depth $\sim$5 μm at 1 GHz). We consider C_{Si} as the equivalent capacitance associated with the Si substrate, which is formed by time-varying fields and is independent of tuning dc bias. Thus, dc tuning of the capacitance of the test structure is caused only by the field-dependent dielectric permittivity of the STO layer. The conductances G_{STO}, G_{SRO} and G_{Si} are associated with the real part of the loss in STO, SRO layers and Si substrate, respectively. G_{STO} is determined by both the dc resistance due to the long range transport of charge carriers (the leakage current) and frequency-dependent resistance due to short range polarization (microwave loses), while G_{Si} value is determined only by microwave losses due to the isolation by CeO_2/YSZ oxides and due to shorting out by the SRO layer.

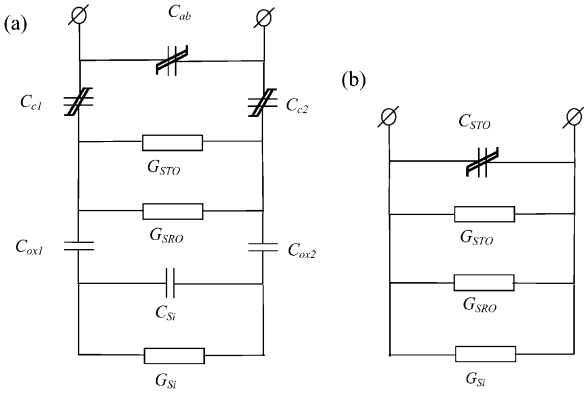

Fig. 3. Equivalent circuit of a $SrTiO_3/SrRuO_3/CeO_2/YSZ/Si$ test structure (a) and its simplified representation used for computational purposes (b).

3.3. Dielectric properties

Fig. 4 presents the typical dc bias dependencies of the capacitance of a $SrTiO_3/SrRuO_3/CeO_2/YSZ$ test structure measured at 10 and 40 GHz. The dielectric permittivity of STO decrease under applied dc field resulting in a corresponding reduction in capacitance. The dependence of the dielectric permittivity of an incipient ferroelectric ($SrTiO_3$) on the applied biasing field can be correctly modelled by solving the Ginsburg–Devonshire equation.[16,17]

Fig. 5 shows the tunability (at 20 V) and zero bias capacitance of the $SrTiO_3/SrRuO_3/CeO_2/YSZ$ test structure and the capacitance of the corresponding CeO_2/YSZ open structure versus frequency. As it can be seen from Fig. 5, the experimental capacitance of both structures in double-log format lie on the straight lines, i.e. dispersions correspond to the Curie–von Schweidler model:

$$\varepsilon = \varepsilon_\infty + k_0\omega^{\alpha-1}, \tag{3}$$

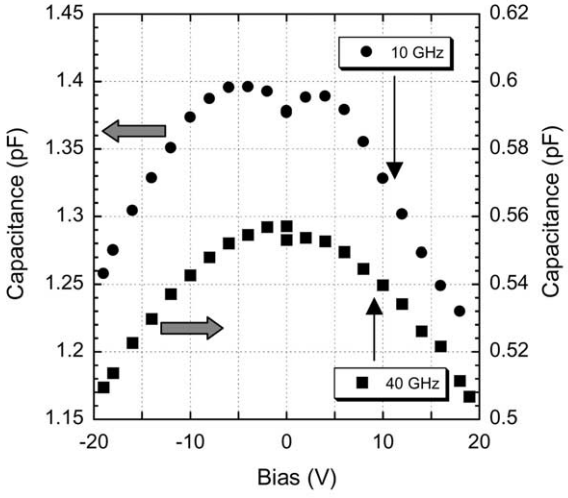

Fig. 4. DC bias dependencies of the capacitance of a $SrTiO_3/SrRuO_3/CeO_2/YSZ/Si$ test structure measured at 10 GHz and 40 GHz.

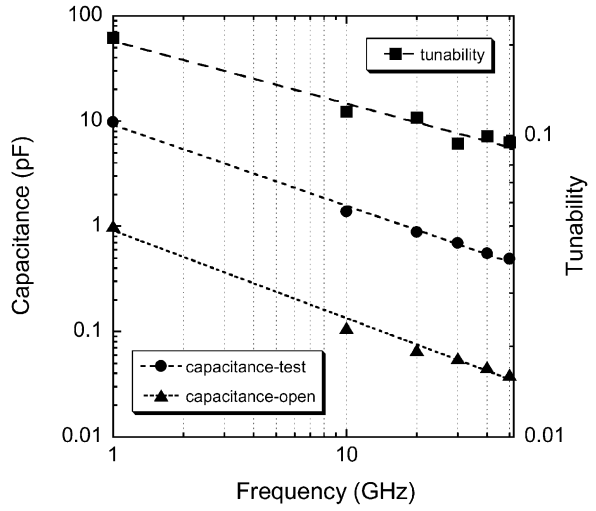

Fig. 5. Frequency dependencies of the tunability (at 20 V) and zero bias capacitance of the $SrTiO_3/SrRuO_3/CeO_2/YSZ/Si$ test structure and $CeO_2/YSZ/Si$ open structure.

where ε and ε_∞ are the real part of the permittivity and its value at very high frequencies, respectively; k_0 and α are parameters.[18] Parameter α is 0.23 and 0.17 for test and open structures, respectively. The capacitance of the test structure is at least 10 times larger then corresponding open structure in all frequency ranges. Hence, the capacitance of the test structure is determined mainly by permittivity of the STO layer.

Fig. 6 shows zero bias loss tangents of the $SrTiO_3/SrRuO_3/CeO_2/YSZ$ test structure and the corresponding CeO_2/YSZ open structure versus frequency. Due to the

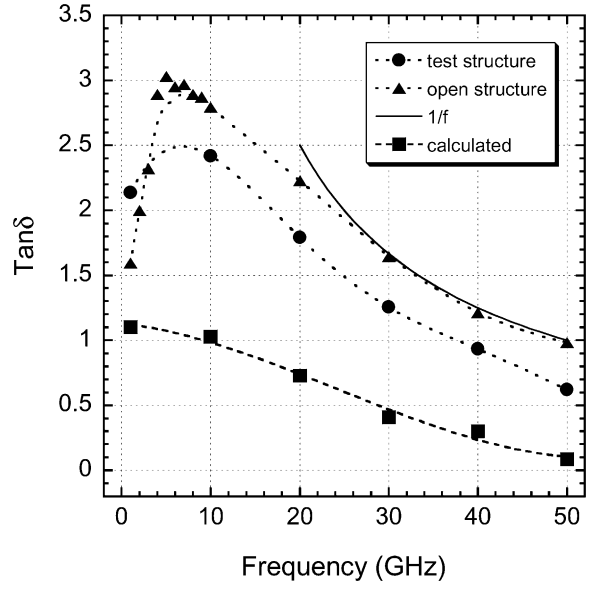

Fig. 6. Frequency dependencies of zero bias loss tangent of $SrTiO_3/SrRuO_3/CeO_2/YSZ/Si$ test structure, $CeO_2/YSZ/Si$ open structure and values calculated for heterostructure excluding losses in Si substrate. The solid line presents a 1/f dependence.

screening effect of high permittivity of STO and $SrRuO_3$ films, the losses in test structure are smaller than that for the open structure. That total losses in the test structure are determined mainly by loss inside the Si substrate. The dielectric dispersion in the Si substrate is characterized by the dielectric (Maxwell) relaxation frequency[19]

$$f_{\mathrm{dr}} = 1/2\pi\tau_{Si} = 1/(2\pi\ \varepsilon_{Si}\ \varepsilon_0\ \rho_{Si}), \tag{4}$$

where τ_{M} is the relaxation time, ε_{Si} and ε_0 are the dielectric constants of silicon and free space, respectively, ρ_{Si} is resistivity of silicon. For our case $\rho_{Si}=25$ Ωcm and $f_{\mathrm{dr}} \approx 6$ GHz, which exactly corresponds to the maximum losses of the open structure (Fig. 6). Besides, according to simple Drude model (Ref. 7), in the frequency range $f >> f_{\mathrm{dr}}$ the loss tangent in silicon may be given as

$$\tan\delta_{Si} = 1/(2\pi f\varepsilon_{Si}\ \varepsilon_0\ \rho_{Si}) = f_{\mathrm{dr}}\ /f. \tag{5}$$

On Fig. 6 the solid line corresponds to $\tan\delta_{Si} = G\, f_{\mathrm{dr}}/f$ (where $G=10$ is a geometrical factor).[7] At frequencies above 30 GHz the 1/f relationship coincides with experimental curve, which also confirms that losses in open structure are mainly due to the Si substrate.

That capacitance of the open structure is much less than the capacitance of corresponding test structure (Fig. 5), which makes it possible to estimate the contribution of the losses due to the Si substrate. In the equivalent circuit [Fig. 3(a)] we can neglect the C_{M} and C_{ox1}, C_{ox2} forming the open structure capacitance. Fig. 3(b) shows the simplified equivalent circuit of the test structure. Here C_{STO} combines the in-plane and out-off-plane capacitance of the STO film. In this case the loss tangent of the test structure is

$$\tan\delta_{\mathrm{test}}\frac{\mathrm{Re}\,Y_{\mathrm{test}}}{\mathrm{Im}\,Y_{\mathrm{test}}} = \frac{G_{\mathrm{STO}} + G_{\mathrm{SRO}} + G_{\mathrm{Si}}}{\omega \cdot C_{\mathrm{STO}}} \tag{6}$$

where ReY_{test} and ImY_{test} are the real and imaginary parts of measured admittance, respectively. Then the loss tangent of structure without loss in Si substrate is

$$\tan\delta_{\mathrm{test}}\frac{\mathrm{Re}\,Y_{\mathrm{test}} - \mathrm{Re}\,Y_{\mathrm{open}}}{\mathrm{Im}\,Y_{\mathrm{test}}} \tag{7}$$

where $ReY_{\mathrm{open}} = G_{Si}$ is real part of admittance of the open structure. The calculated values of tanδ are presented in Fig. 6. It can be seen that at frequencies up to 50 GHz the tanδ values go down to 0.08.

4. Conclusions

High quality $SrTiO_3$ layers (FWHM = 0.95°) with buffer $SrRuO_3/CeO_2/YSZ$ thin film structure have been

grown on low-resistivity (25 Ω cm) Si(100) substrates using a laser ablation technique. The frequency dispersion of the $SrTiO_3$ dielectric constant is described by the Curie–von Schweidler model. The tunability of capacitance is larger than 10% and the calculated loss tangent (without losses in silicon) of 0.08 at 50 GHz makes this capacitor test structure promising for application in tunable microwave devices. The parasitic influence of the Si substrate in such devices can be cancelled by micromachining-forming a cavity in Si under the device,[8] or increasing the conductivity and thickness of buffer $SrRuO_3$ layer in order to prevent the electric field penetration into the Si substrate.

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